L'électronique de spin (spintronique) : une solution d'avenir pour un numérique frugale (?)

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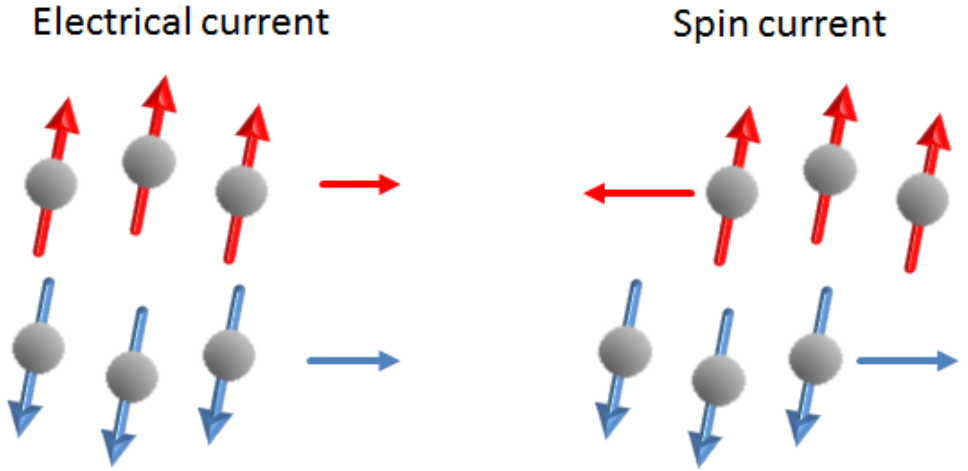
OUTLINE

- La Spintronique et ses applications phares
- Les challenges de la mémoire embarquée
- Des solutions spintronique pour le numérique de demain
- Conclusions

Qu'est ce que la spin-*elec*-tronics?

Spintronics – make use of **intrinsic quantum property of electrons (spin)** as additional degree of freedom for new electronics

electron



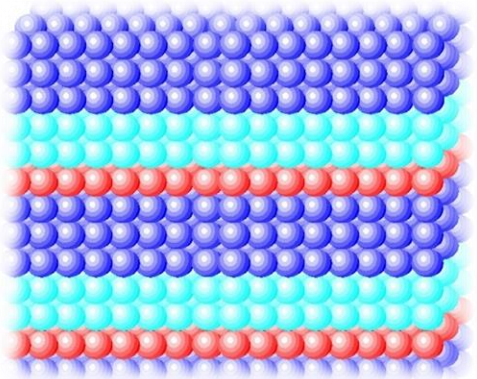
Ultralow power consumption (pJ - aJ)

$E = R I^2 \Delta t$

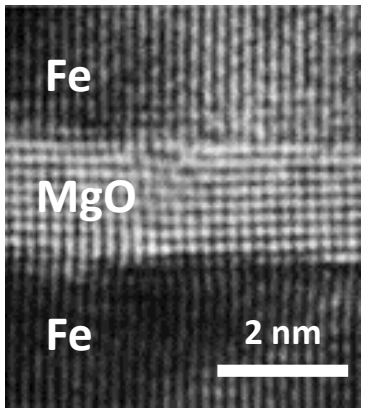
Ultrafast dynamics (ns - fs)

Materials engineering at nanoscale range

Magnetic multilayers

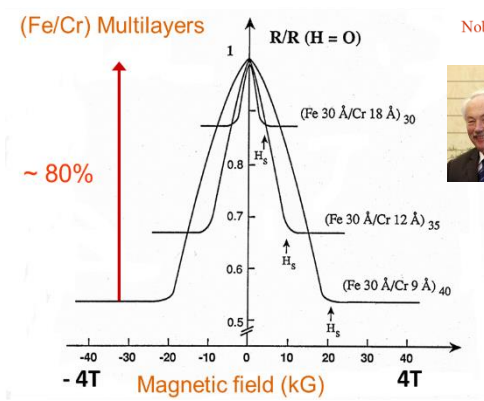


Cross-section image of a multilayer

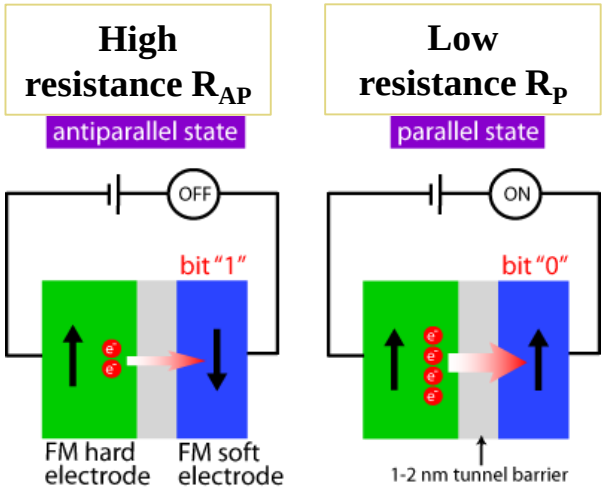


Combined to currents

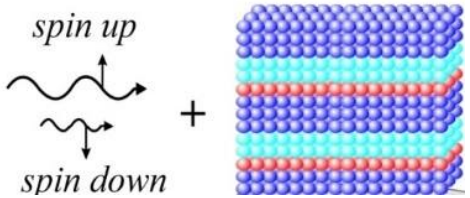
Large magneto-resistance signals

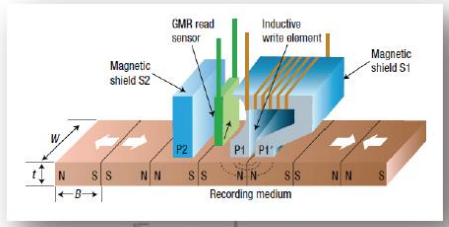


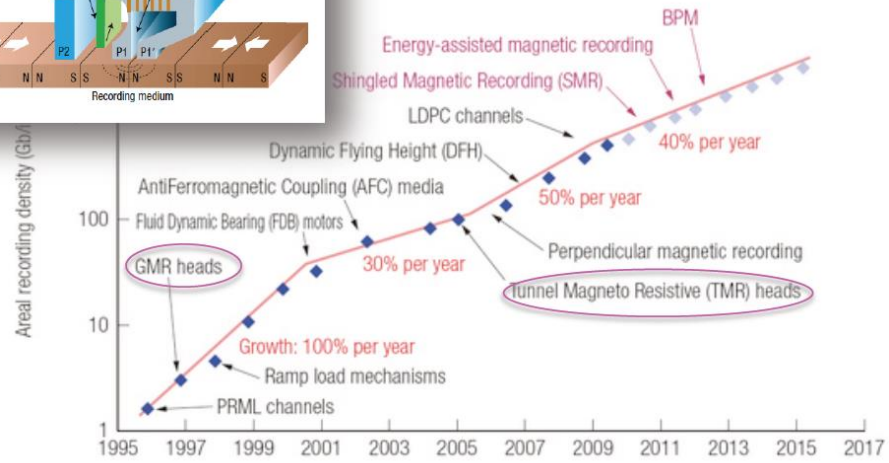
Gives sensor / memory device



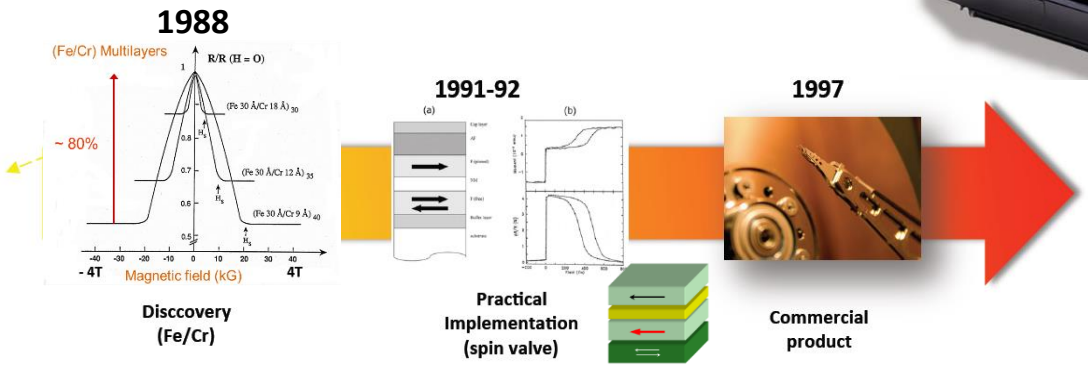
1st revolution : *magnetic recording and sensors*



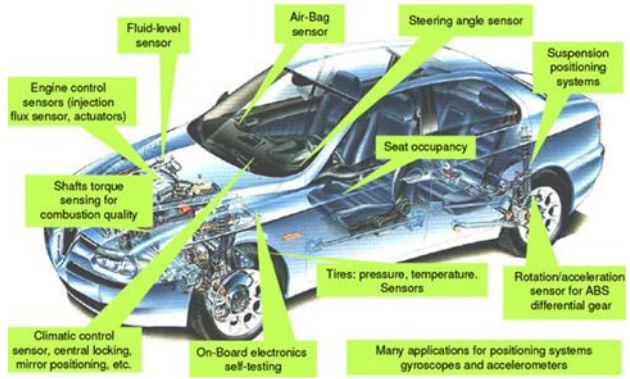




Still a growing market nowadays (mostly for server farms

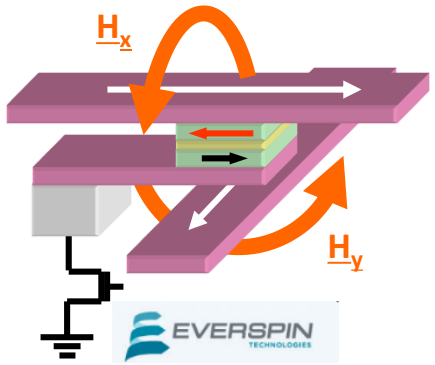


Direct impact on market with magnetic field sensors
Today in MEMS, minimally invasive surgery, Automotive sensors, Anti-skid system, speed control and navigation...

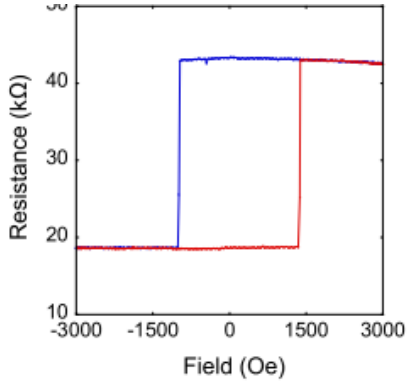


2nd ongoing revolution : *MRAMs*

Field-driven MRAM

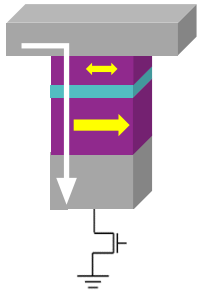


Toggle MRAM

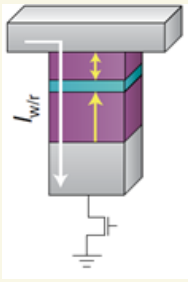


Current-driven MRAM

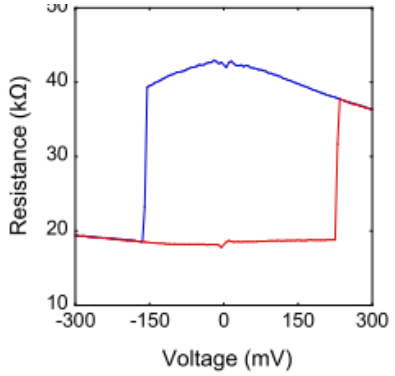
Planar



Perpendicular



Spin transfer torque (STT)

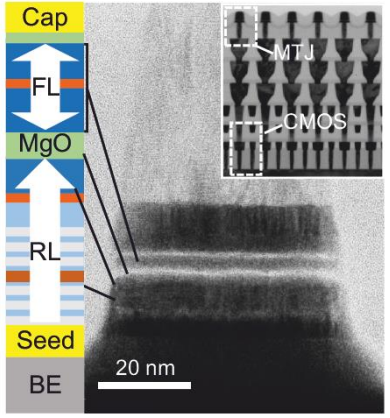


Brique de base: jonction tunnel magnétique (MTJ)

Lecture : TMR (tunnel magneto-resistance)(~ 200%)

Ecriture: STT → Convertir charge en spin via un matériau ferromagnetique + transférer un couple

→ STT-MRAM = Un contrôle toute électrique



Stockage: FL (>10y)

Stack MRAM moderne

- **8 compounds**
- **sub-nm layers**
- **> 20 layers**
- **Supporte 400C**

Mais des matériaux « critiques »: Ta, Pt, Ru, Co…

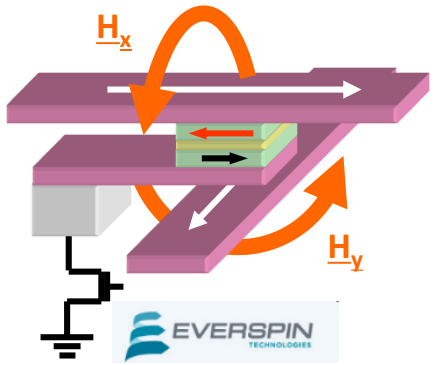
→ projet NEED pour minimiser/substituer ces matériaux

NEED for IoT
Univ. Grenoble Alpes

2nd ongoing revolution : *MRAMs*

Legacy | **Maturity, production**

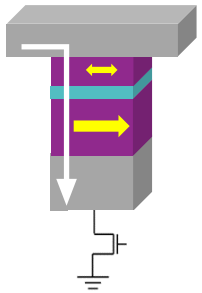
Field-driven MRAM



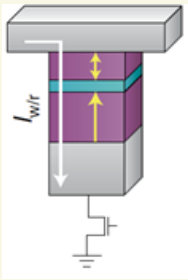
Toggle MRAM

Current-driven MRAM

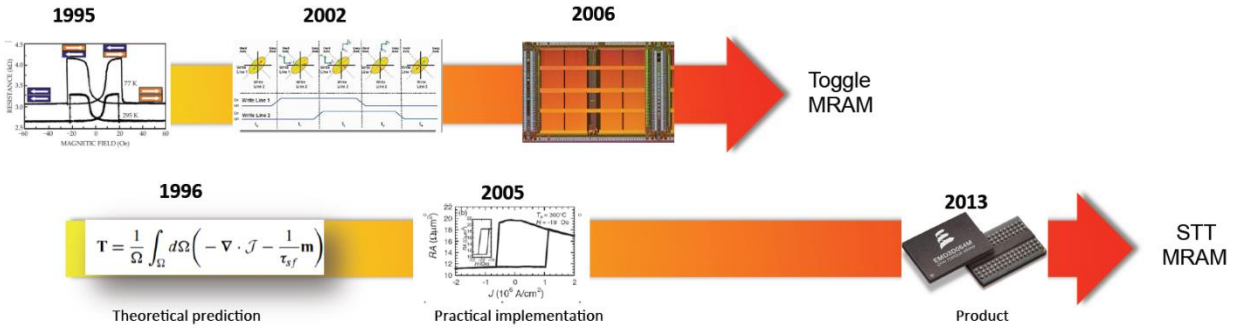
Planar



Perpendicular

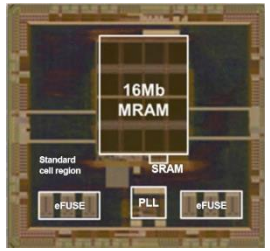


Spin transfer torque (STT)



But only for standalone

Since 2012, major actors of semiconductor-foundries, IDM, tool suppliers active for embedded MRAM



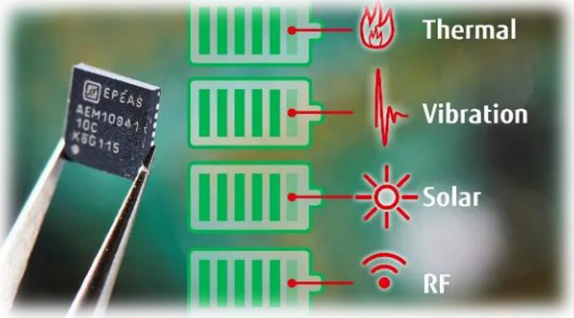
MRAM: un stack, de multiples opportunities µelec

Spintronic & FD-SOI for Ultra-low power
Mobile applications, server clusters, HPC, beyond CMOS

IoT, 5G : RF devices, telecoms, wake-up receivers

Field / position / speed sensor - **automotive, IoT**

Spintronic Neural Networks
Artificial Intelligence

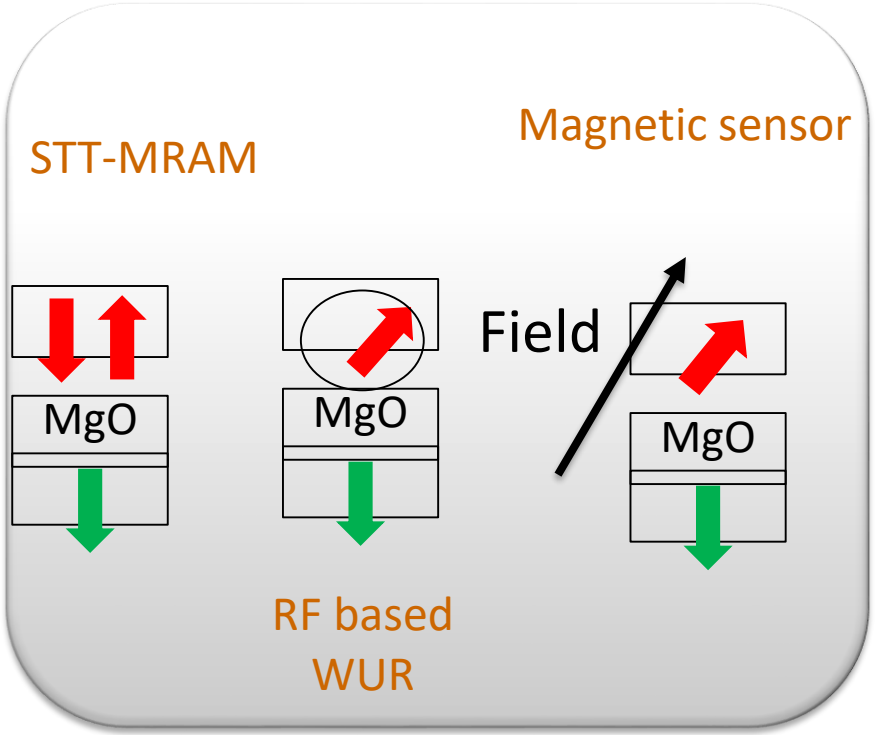


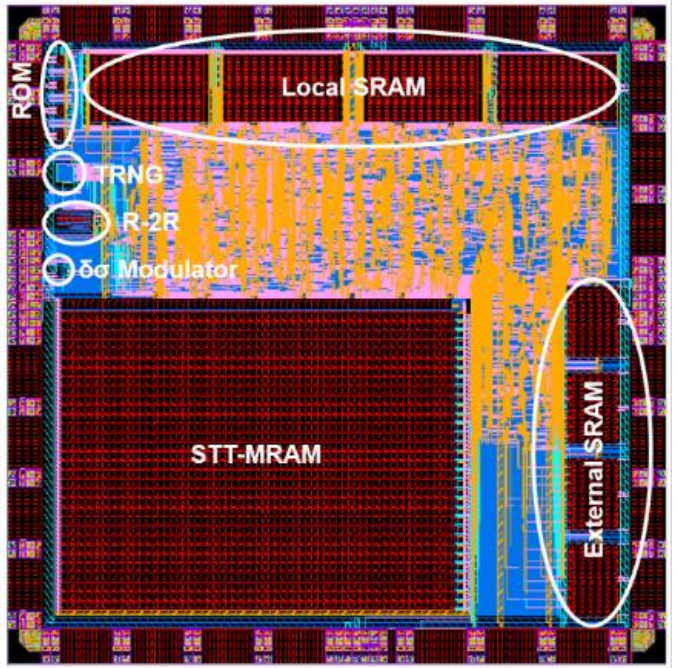
Energy harvesting
Temperature gradient (*spin-Seebeck)*
Ambient electromagnetic radiations *(spin-diodes)*

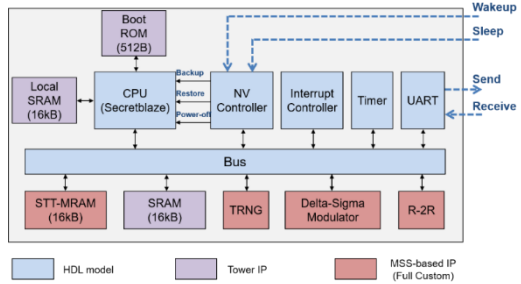
Hardness to radiations-
Defense, nuclear & aerospace

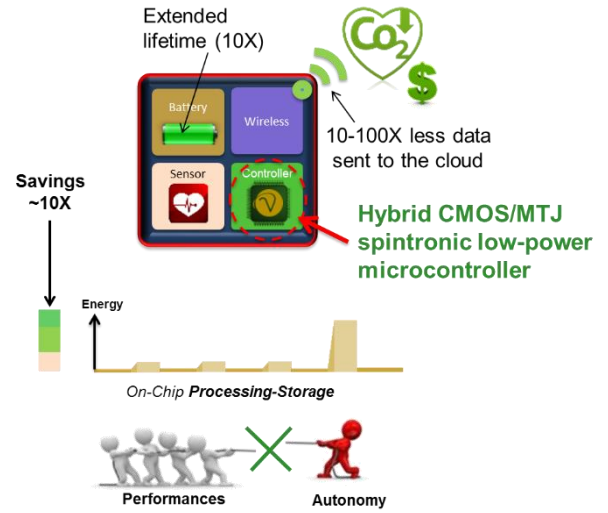
An “all” spintronics plateform opportunity

Three functionalities with same magnetic stack for **Internet of Things allowing memory, sensing and RF on the same die**









- **Design of a 128kb memory array, compiler compatible**
- **First demonstration of a magnetic microcontroller embedding analog and digital functionalities**

OUTLINE

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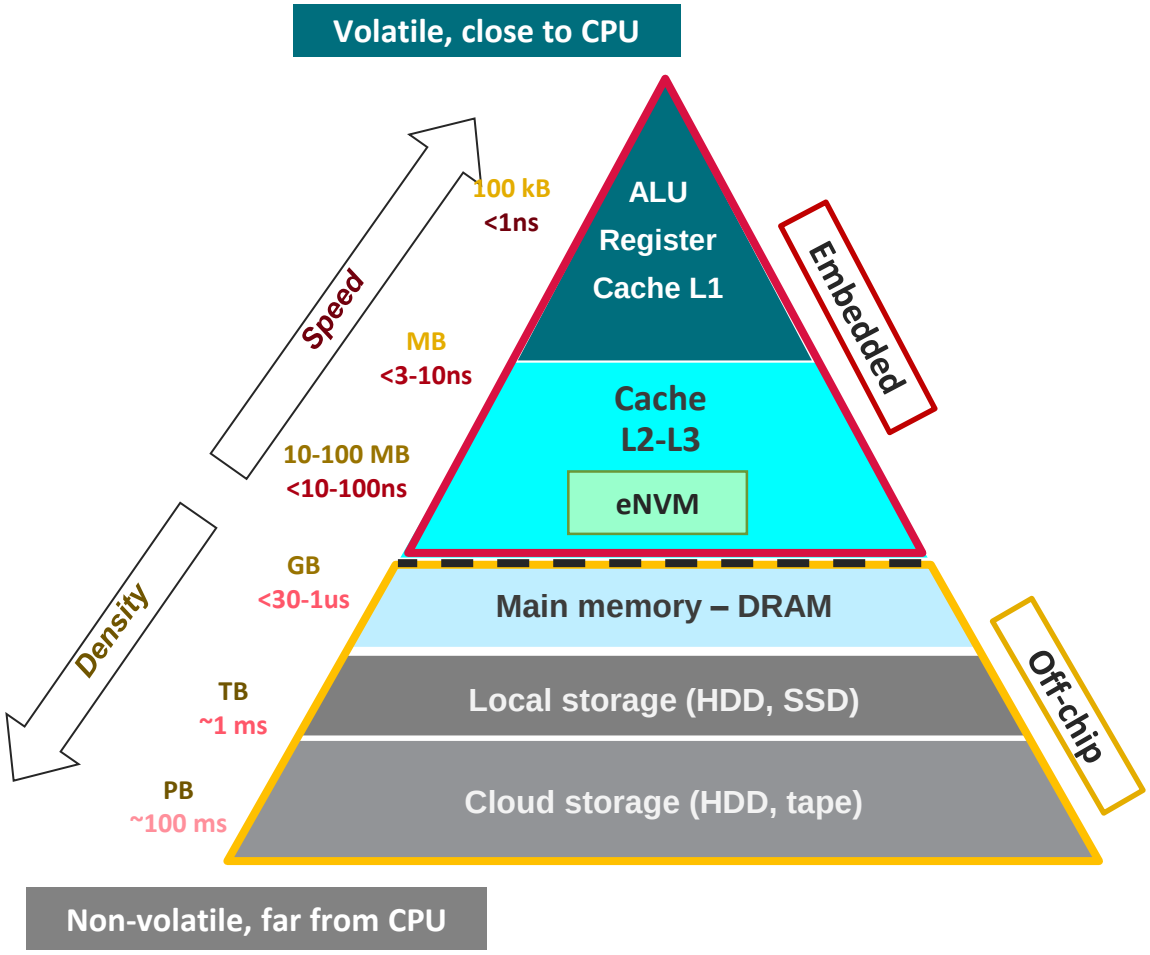
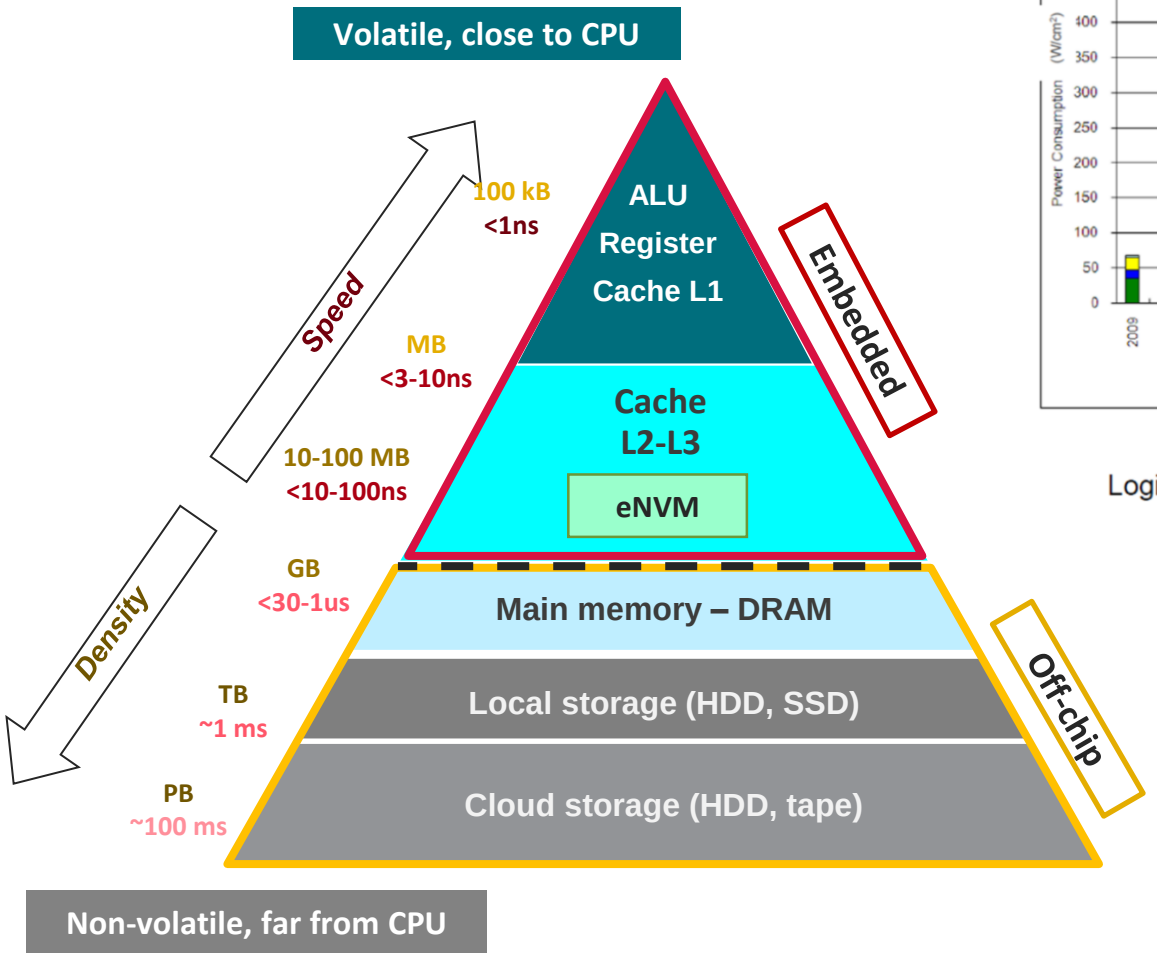
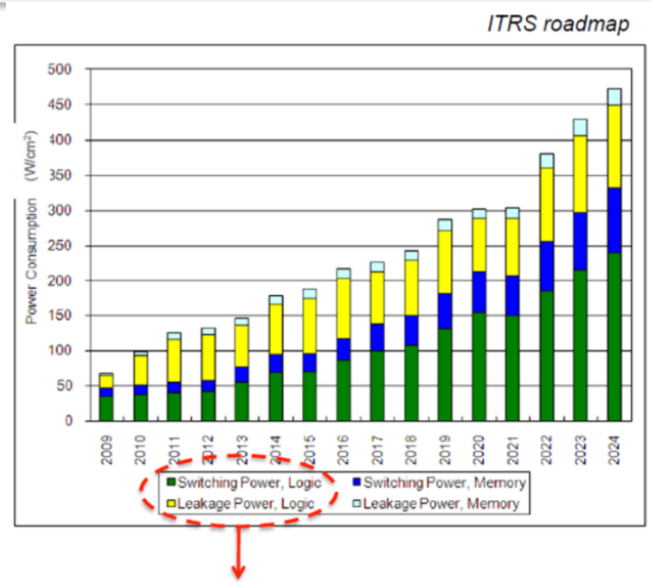
Hiérarchie mémoire



Hiérarchie mémoire et impact du scaling





Logic is the major issue !

Conséquences de l'ultra scaling :

- Courant de fuite > courant écriture
- Augmentation coût de production
- Problèmes de fiabilité

→ **Introduction mémoires non-volatiles pour calcul faible puissance et on/off instantané**

Introduire les technologies NVM dans le cache

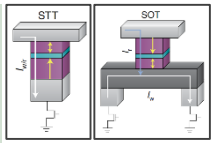
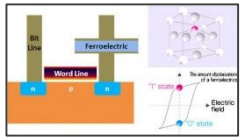
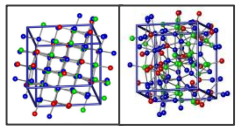
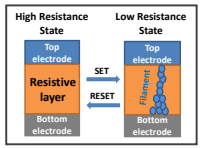
Augmentation la taille du cache
→ Réduire la dépendance DRAM

Revisite de l'architecture système
→ Gain de vitesse, puissance, efficacité
→ Développement de nouveaux concepts de calcul

Les technologies mémoires non volatiles

Introduire les technologies NVM dans le cache
= être compétitif avec la SRAM:

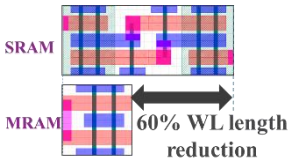
~1ns, 10^{16} cycles, fJ

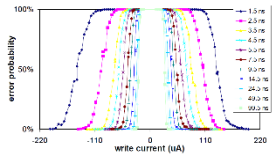
		Électroniques		Ioniques	
	Mémoire CMOS (volatile)				
	SRAM	**MRAM**	**FeRAM Fe-FET**	**PC-RAM**	**RRAM**
V_{DD}	<1.1V	<1.1V	2V	3-5V	1.5-3.6V
Surface	**1**	**0.4-1**	**0.4-1**	**0.4**	**0.4**
Rapidité	**ns**	**ns**	**20ns**	**100ns**	**100ns**
Energie/bit	fJ	<pJ	**10fJ**	10pJ	10pJ
Endurance	**>10^{16}**	**10^{14-16}**	**10^{12}**	**10^{8}**	**10^{6}**
Hiérarchie mémoire	Registre Cache	Cache **eFLash**	eFlash Autonome	eFlash Autonome	eFlash Autonome
Calcul IMC	ANN, Boolean, Learning	ANN, Boolean, Stochastic	ANN	ANN	ANN

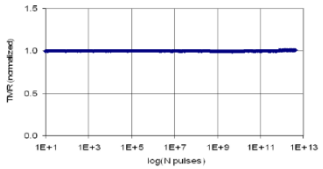
Les mémoires **magnétorésistives** et **ferroélectriques** mieux placées pour besoins de l'embarqué et du calcul

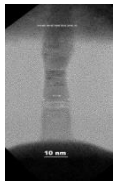
La MRAM a des atouts à faire valoir

- CMOS compatible (V_{sw}<V_{dd}, BEOL)
- Fast (ns) & Endurance (>10^{12})
- Scalable & dense









MRAM *in production for embedded Flash replacement*

STT-MRAM for Microcontrollers products

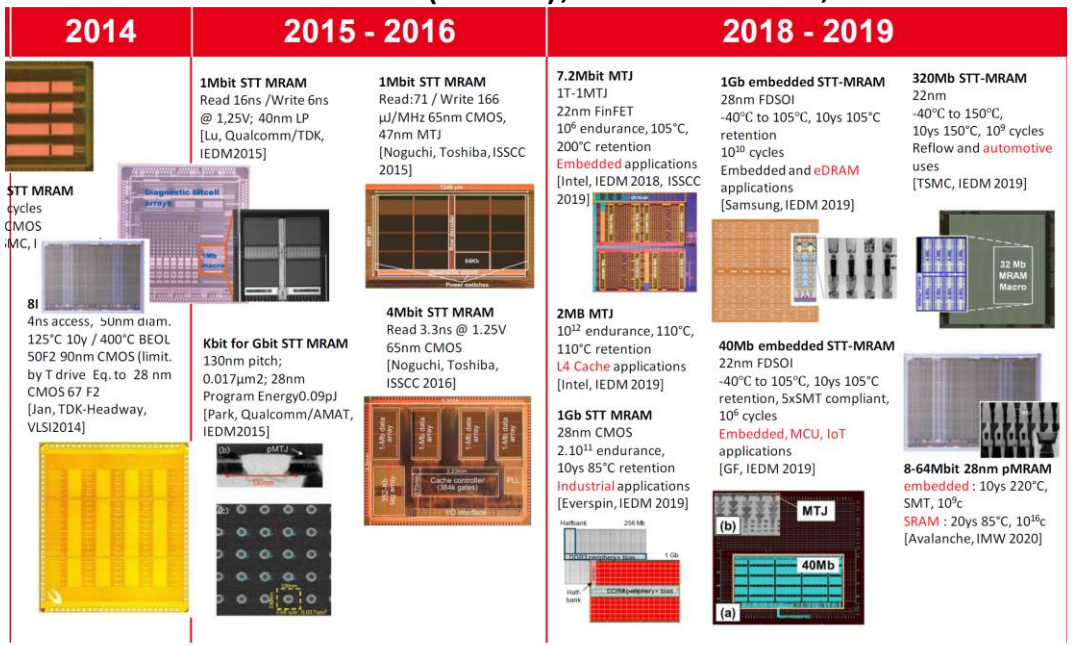
→ 3 levels of masks vs. 15-20 masks for eFlash

→ better endurance (>10^{12} vs 10^{5})

→ faster write (40ns vs 100ms)

→ reduced energy (400x reduction @ device)

Markets: Automotive (>50%); Smart Cards; Consumer



First usage case are on the market

Product 1 – Sony

Source: Huawei

- Sony's GNSS/GPS SoC (CXD5605) is based on a Samsung S4LP173 die manufactured on 28nm FDSOI that features 8Mb of eMRAM.
- Sony's CXD5605 chips are utilized in low-power Huawei Watch GT2. They were first introduced at the FDSOI Shanghai Forum in September 2019.

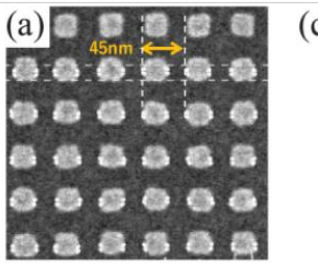
Product 2 – Ambiq Micro

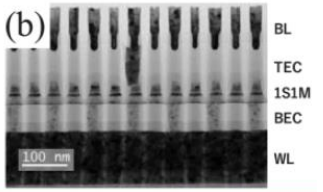
Source: Ambiq

- In September 2020, Ambiq launched the 4th series of Apollo MCUs, which employ 16Mb **eMRAM** instead of eFlash. They are manufactured with TSMS's 22nm ULL process.
- Apollo 4 MCUs are based on Arm Cortex-M4, which runs up to 192 MHz while using 3 µA/MHz (10 times lower than the industry average).
- The Apollo family of highly-integrated MCUs from Ambiq Micro are optimized for use in **wearable electronics, activity & fitness monitors, wireless sensors** and other **power-sensitive and battery-operated applications**.

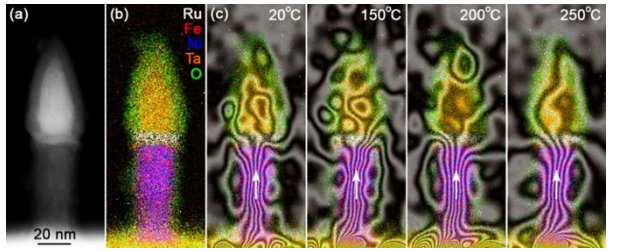
Remaining limitations in STT-MRAM technology :

Hynix, https://ieeexplore.ieee.org/document/10019549





- **Write speed : tradeoff speed/endurance**
- High capacity: patterning at small feature size and narrow pitch
- Thermal stability at sub-20nm node and elevated temperatures



K. Watanabe et al., Nature com (2018)
N.Perrissin et al., Nanoscale 10, 12187-12195 (2018)

MRAM vs. SRAM pour LLC: écrire plus vite, à moindre cout

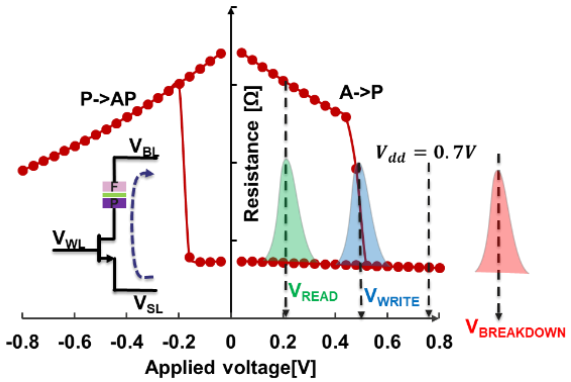
Vitesse écriture par STT :

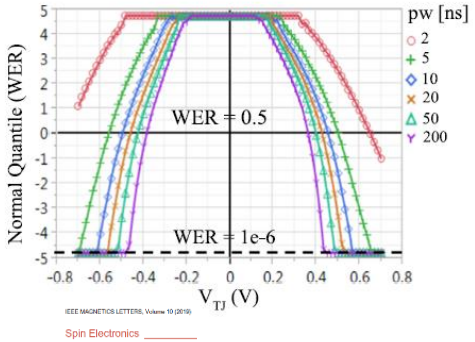
Compromis écriture/endurance

endurance vs. τ_{write} → Write latency > 10-15ns

<u>Introduire MRAM in LLC:</u>

→ Géométrie alternative, autre mécanisme écriture

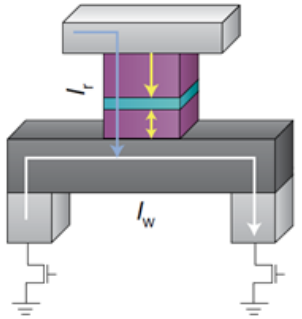


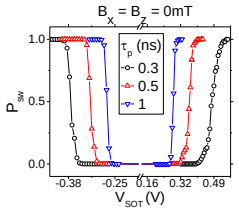


Speed, advanced R&D

Low power & fast, early R&D

<u>Spin-orbit torque (SOT)</u>

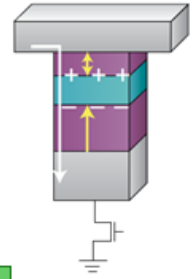


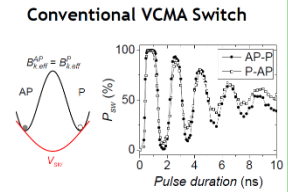


200 ps, 100 fJ, 3T

- Convertir charge en spin dans matériaux non FM
- Découplage écriture/lecture
  - "unlimited" endurance
  - No read disturb

<u>Voltage control of anistropy</u>
(VCMA)





500 ps, 10-100 fJ, 2T

- Contrôle anisotropie par tension
- Exploite dynamique aimantation
- Ecriture unidirectionnel

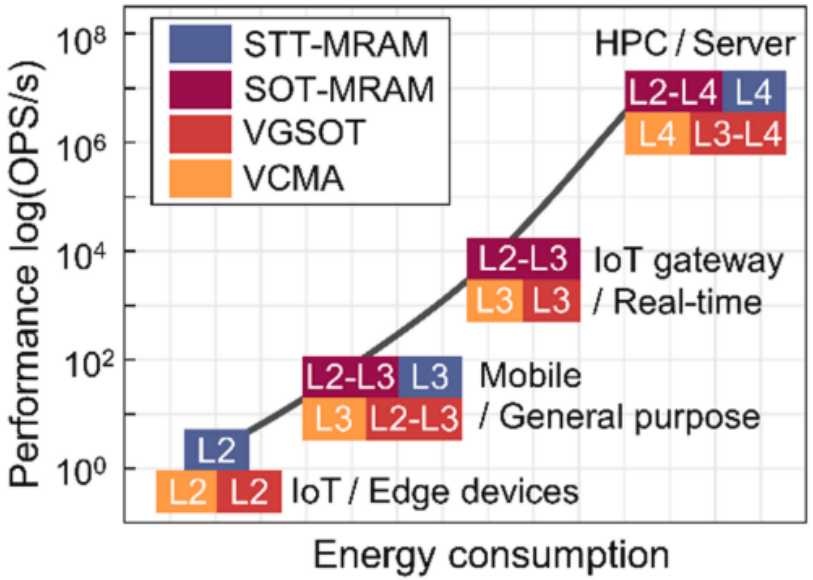
📖 Dieny et al, Opportunities and challenges for spintronics in the microelectronic industry, Nature Electronics 3, p. 446–459 (2020)

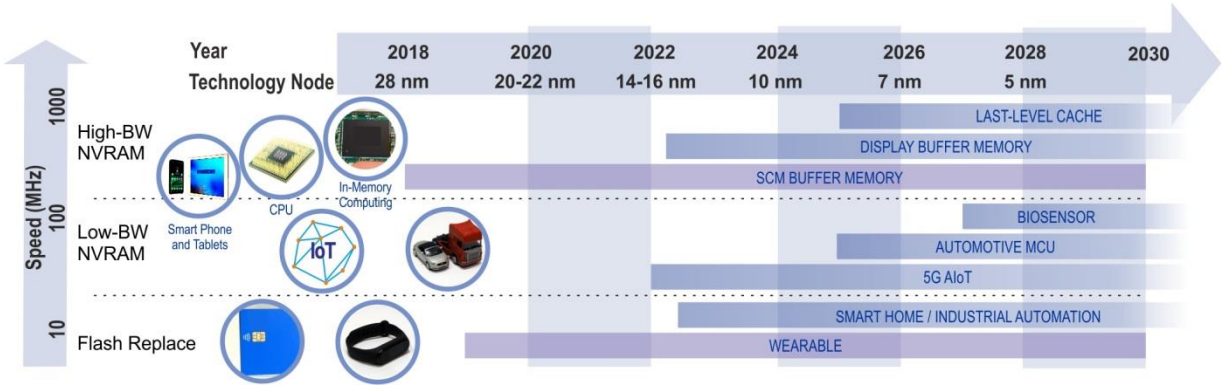
Quelques projections des techno MRAM émergentes

Comparative table of potential embedded memory solutions at the macro level (5 nm node, 128 kbit) based on IMEC internal evaluations.

Specs	Embedded memory options									
	SRAM		STT		SOT			VCMA	VGSOT	
	HP (1 2 2)	HD (1 1 1)	HP (1.5 CPP)	HD (2 CPP)	5 T	HP (4 T)	HD (4 T)		2MTJ	4MTJ
Bit-cell area (μm^2)	0.028	0.021	0.0108	0.0081	0.0162	0.0162	0.0135	0.0208	0.0122	0.009
RD power/bit (nW)	18.7	7.28	7.44	6.20	25.5	29.0	32.9	3.16	3.16	2.96
WR power/bit (nW)	25.7	9.85	29.2	24.4	31.4	34.7	35.3	59.2	47.5	46.5
RD latency (ns)	~ 0.80	~ 1.50	~ 2.89	~ 3.75	~ 1.00	~ 1.00	~ 1.00	~ 10.0	~ 10.00	~ 10.00
WR latency (ns)	~ 0.80	~ 1.50	~ 7.78	~ 20.00	~ 2.00	~ 1.40	~ 2.00	~ 1.00	~ 1.00	~ 1.00
Endurance	10^{16}	10^{16}	10^{7}	10^{9}	10^{14}	10^{14}	10^{14}	10^{14}	10^{14}	10^{14}
V_{DD} (V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	1.4	0.7	0.7

Projection de champs d'applications possible





(industrial vision, focused on STT-MRAM)

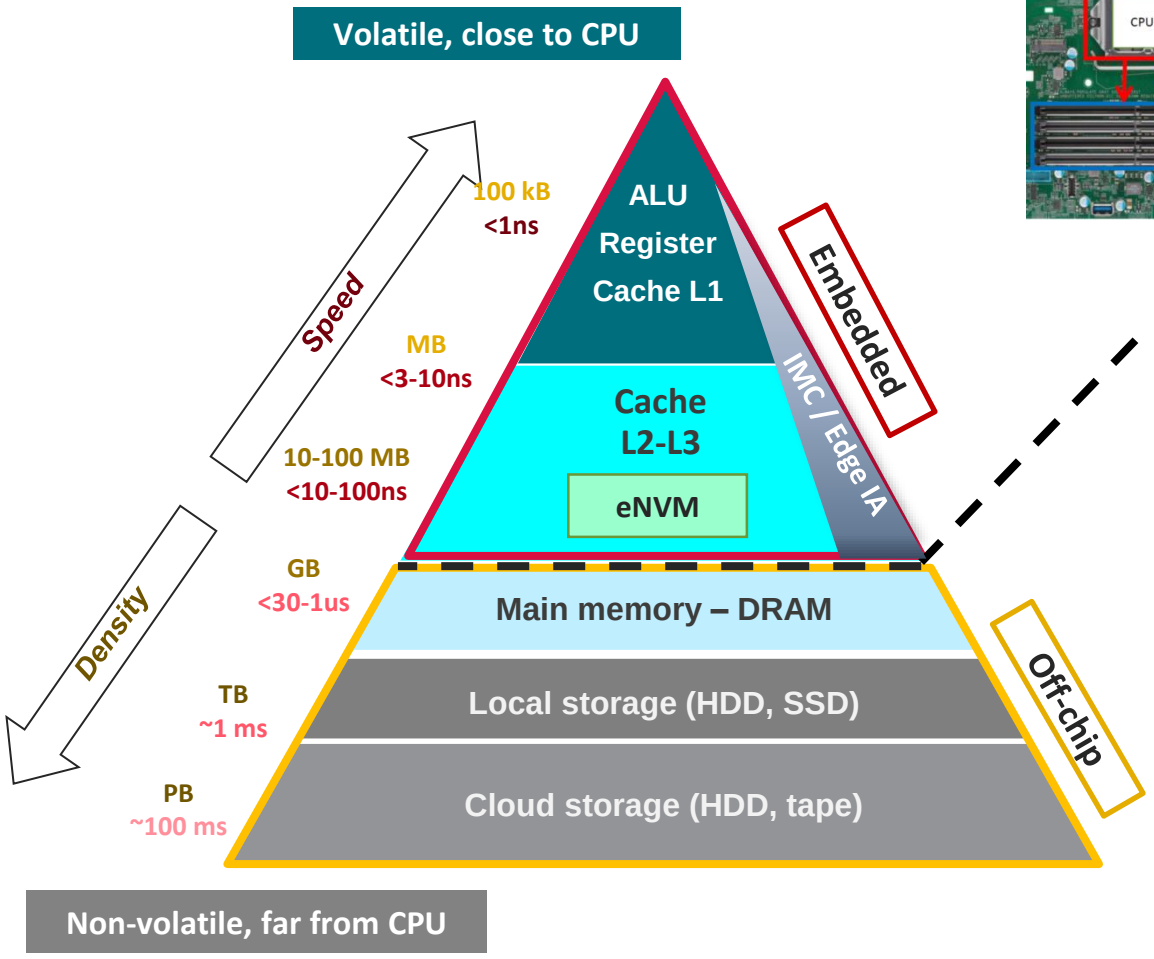
V. Krizakova, KG *et al.*, *JMMM* 562, p. 169692 (2022)

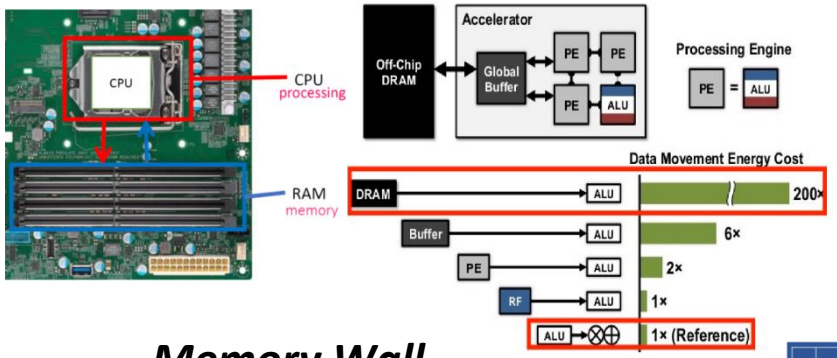
H. Yang et. al, Two-dimensional materials prospects for non-volatile spintronic memories. Nature 606, 663–673 (2022)

OUTLINE

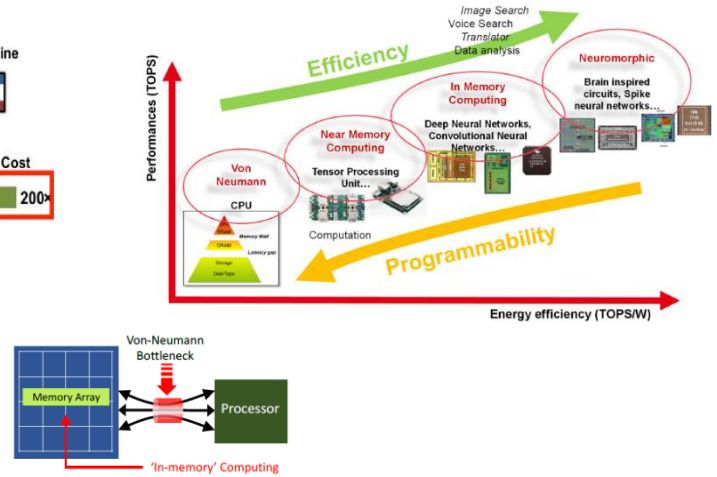
- La Spintronique et ses applications phares
- Les challenge de la mémoire embarquée
- **Des solutions spintronique pour le numérique de demain**
- Conclusions

Memory wall: Vers In-Memory et Edge computing





Memory Wall



L'utilisation de données explose, les contraintes énergétiques apparaissent

⇒ **Traitement local de l'information:**
In- & Near-Memory Computing

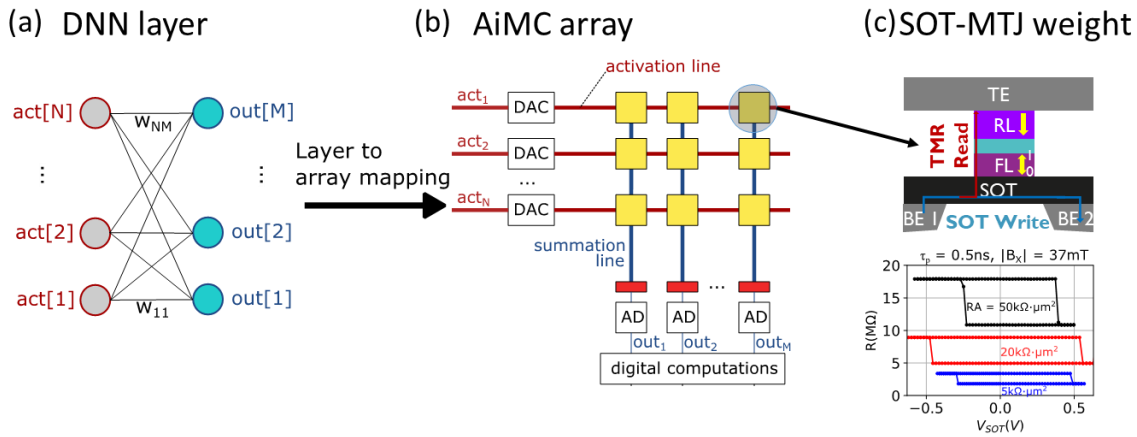
- ✓ Perform logic operation inside memory
- ✓ Parallel, local data processing
- ✓ Low energy, programmable
- ✓ MRAM benefit: increased cache density

G. Mola, Advances in Emerging Memory Technologies: From Data Storage to Artificial Intelligence. *Applied Sciences* **2021**, *11* (23)

Au delà des mémoires: nouveaux paradigmes de calcul

In-memory computing

- Analog-iMC: DNN/SNN inference
  Sort and Recognition (image, speach…)
- High Resistance is key → exploit third terminal → SOT



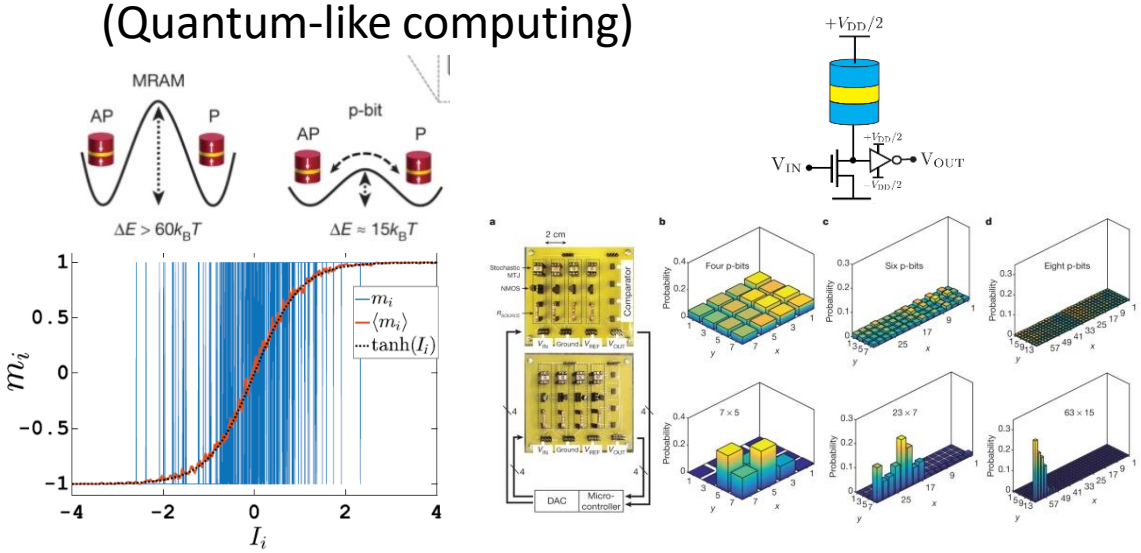
J. Doevenspek, et al, VLSI 2020, JFS4.1 (2020), S. Jung, et al. A crossbar array of magnetoresistive Nature 601, 211–216 (2022)

Assests MRAM for emerging computing

- Low variability cell-to-cell
- Tunable properties: retention, resistance
- Speed

Stochastic /probabilistic computing

- Ising, Bayesian, pBit
  Factorization, full adder… functionalities
  (Quantum-like computing)

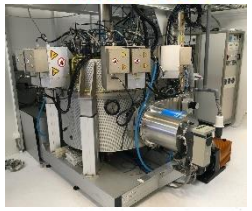


W. Borders et. al, Nature v573, pages390–393 (2019), Fukami et. al, NatureCom (2020)
Grollier, J., Querlioz, D., Camsari, K.Y. et al. Neuromorphic spintronics. Nat Electron 3, 360–370 (2020)

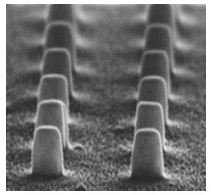
SPINTEC : Aller vers des démonstrations de concepts

Une chaine d'expertise complète

Materials

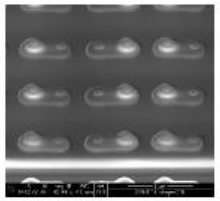


Processing

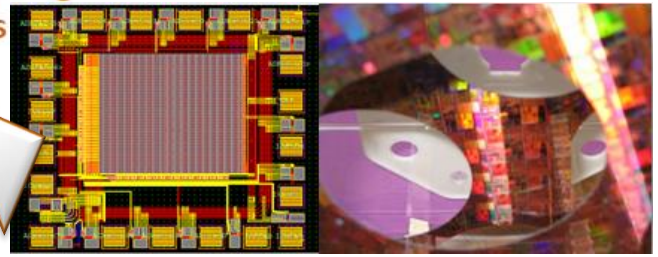


Test at cell level

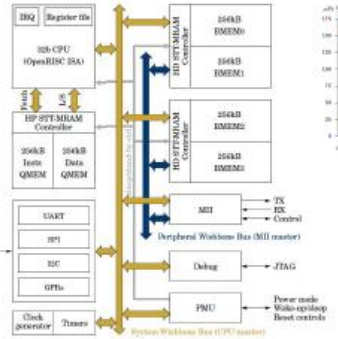
CMOS/magnetic integration



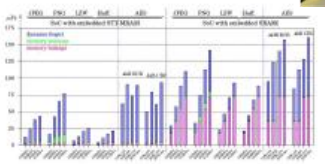
Complex hybrid CMOS/magnetic circuits

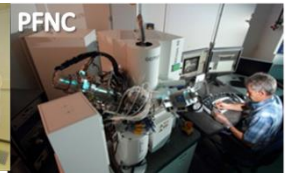


Analog and Digital Circuit Design

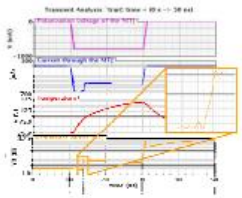


System performance evaluation

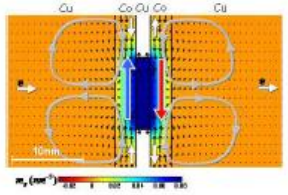




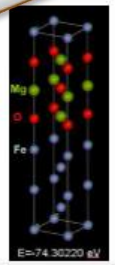
Design tools



Spin-transport and micromagnetism

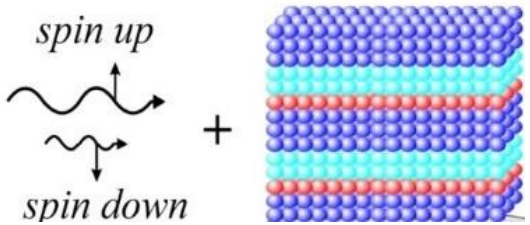


Ab-initio theory



cea 21A1 + 2A2 — cnrs 9 chercheurs, 10 I — UGA Université Grenoble Alpes 1Prof + 2MdC — GRENOBLE INP UGA 2 Profs

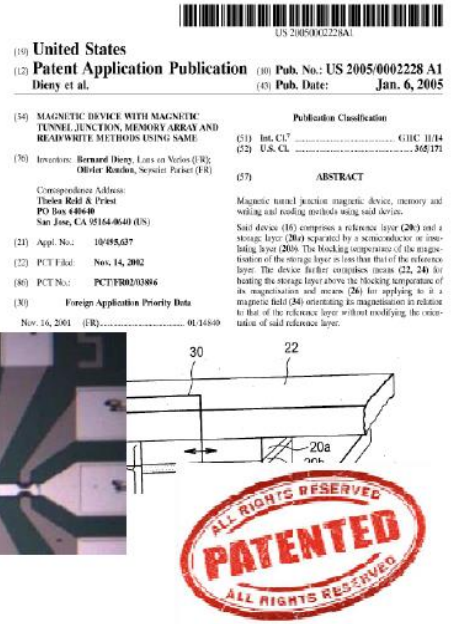
A propos de SPINTEC : nos missions

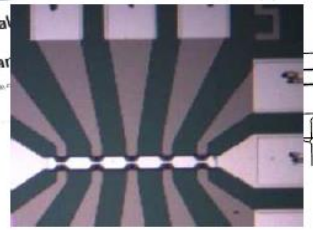


Explore the frontiers of spintronics → Invent new devices paradigms → Transfer technology to partners

Basic research

Applied Research





Valorization/exploitation

CROCUS TECHNOLOGY — Intelligence in Sensing — Magnetic field sensors and MRAM

eVaderis — Design of hybrid CMOS/magnetic circuits

Hprobe — Electrical probers for magnetic memories

antaios — Spin-Orbit-Torque memories

Projet PEPR : EMCOM (mémoires émergentes pour le calcul embarqué)

DEFI

Calcul embarqué performant et économe en énergie

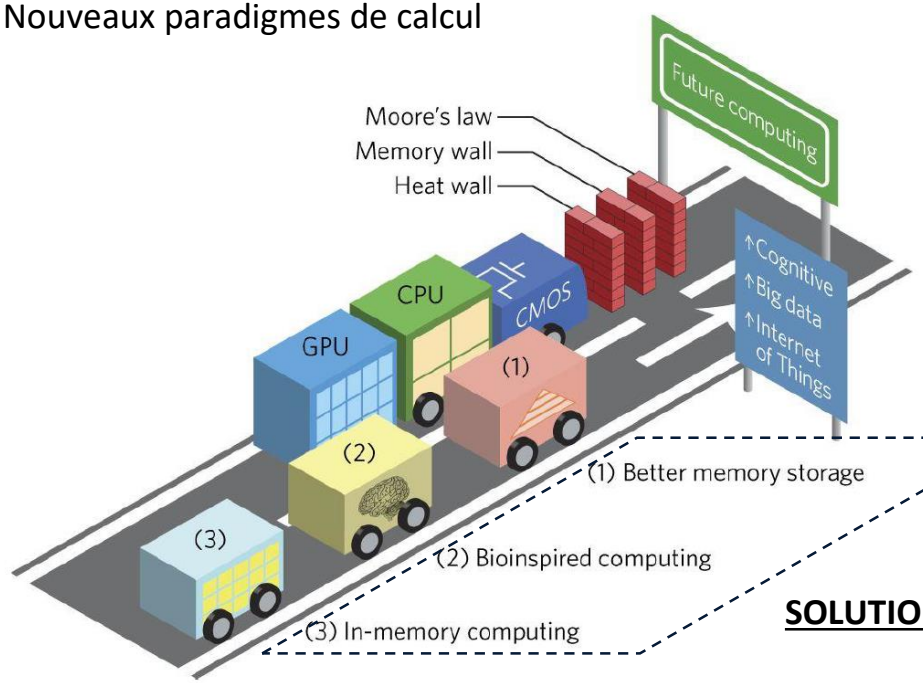
VERROUS

Moore's law, Memory wall, Heat wall

Vitesse d'écriture, très faible énergie, endurance

Architectures innovantes

Nouveaux paradigmes de calcul



(figure adaptée de Yole Development)

SOLUTIONS

(1)

VG-SOT (WP2)
rapide, endurante, multi-niveau
SPINTEC
LETI, C2N, UMPHy, IJL

FESO (WP3)
ultra faible énergie
UMPHy
SPINTEC, LETI, C2N

Optique (WP4)
ultrarapide, faible énergie
IJL
SPINTEC, LTM, C2N

Neuromorphique (WP5/6)
nouveaux paradigmes de calcul
LETI
SPINTEC, C2N, UMPHy, IM2NP

(2)

(3) **Benchmark, spécifications, architectures (WP1)**

Vers une filière nationale *MRAM / calcul embarqué*

- **Matériaux (WP2-WP5)**
- **Nanofabrication (WP2-WP5)**
- **Caractérisation avancée (WP2-WP5)**
- **Architectures (WP1)**

CONCLUSIONS

- **La STT-MRAM constitute la 2nd application majeur de la spintronics** après les capteurs de champs magnétique (particulièrement pour HDD).

- **STT-MRAM est en phase de production en volume** (Samsung, TSMC, Global Foundries, INTEL).

  - **Marque l'acceptation de cette technologie CMOS/magnétique par l'industrie microélectronique**
  - **Première application: Remplacement de Flash embarquée**
  - **En développement: Last level Cache** and memory persistantes (empreinte cellule < SRAM + non-volatile).
    SOT-MRAM et VCMA semblent mieux adresser ce sujet

- **Les propriétés MRAM** peuvent adaptées aux specs des applications (résistance, rétention…)

→ D'autres applications de la MRAM sont attendues dans le domaine de **AI, In-memory computing, ultralow power electronics, IoT, High Performance Computing (HPC), cryoelectronics**… mais des progrès matériaux / concept / architectures sont nécessaires → PEPR EMCOM

ANR-22-PEEL-0009

Merci pour votre attention!

www.spintec.fr

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